

Fig. 1

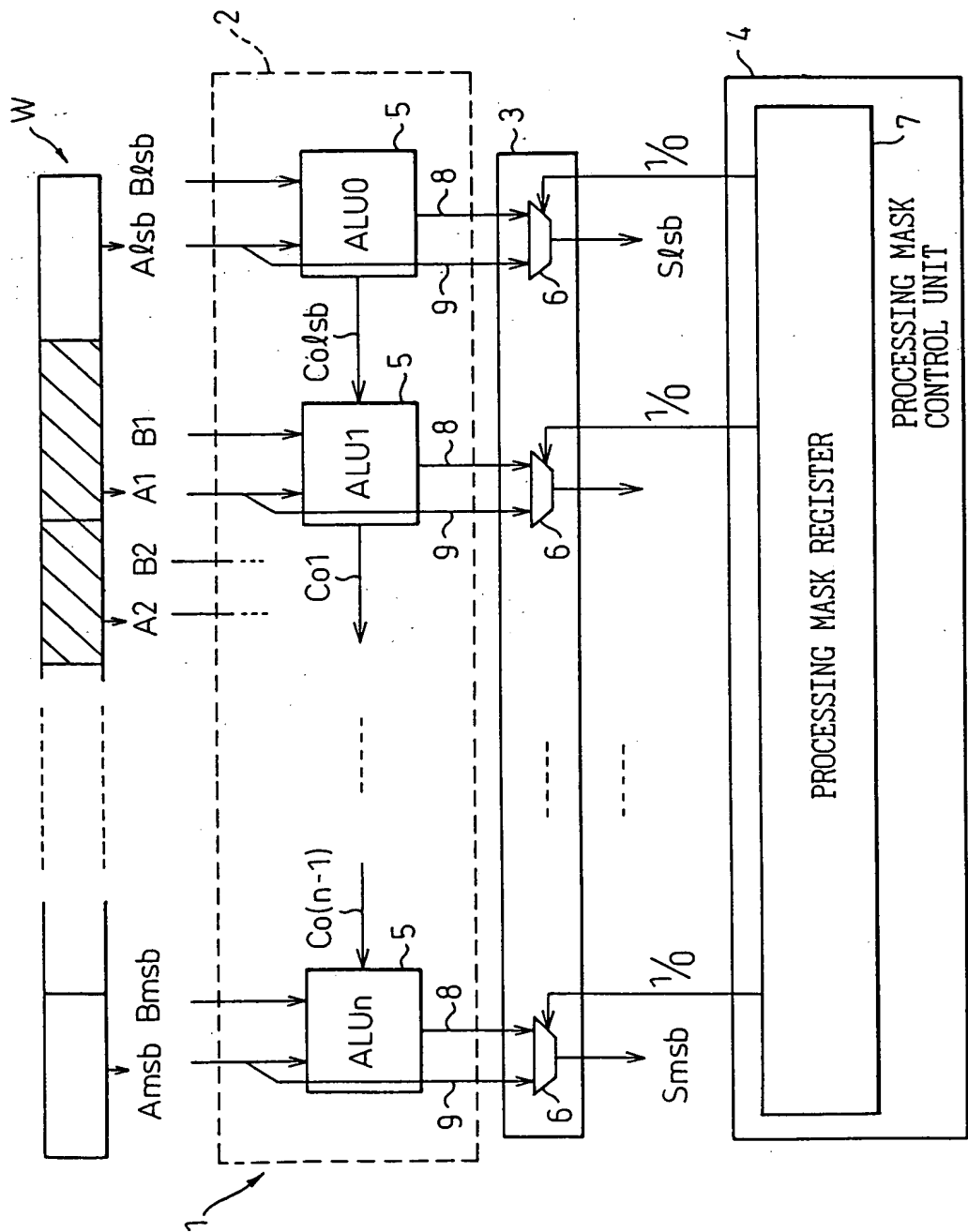


Fig.2

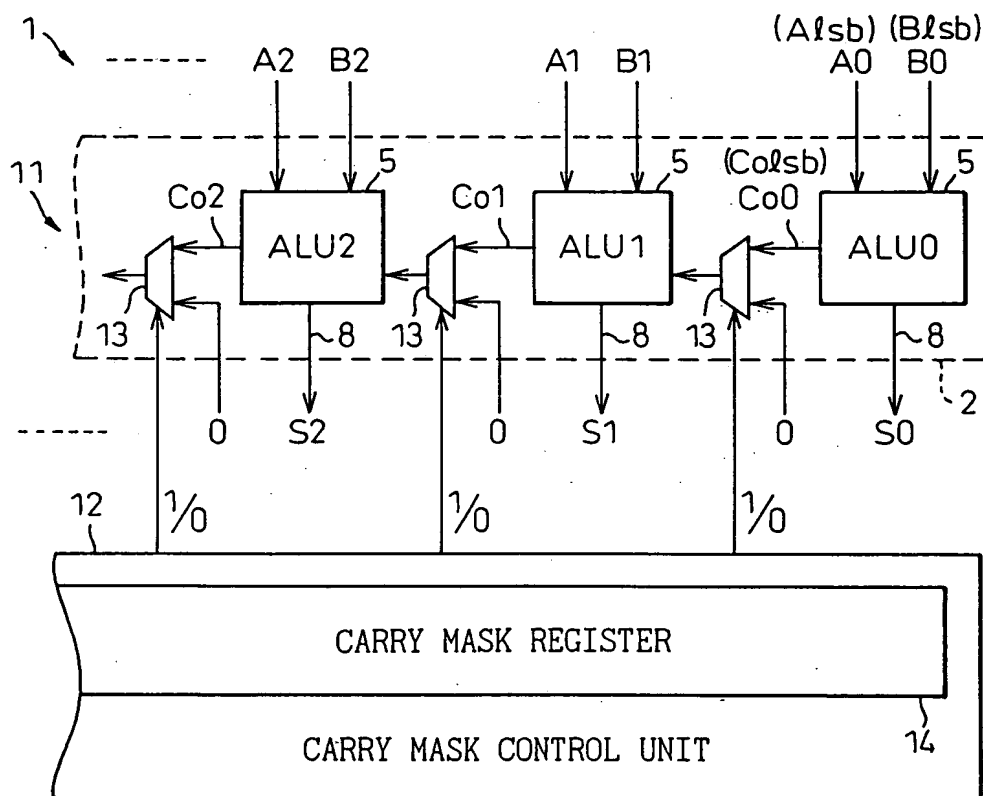




Fig.4

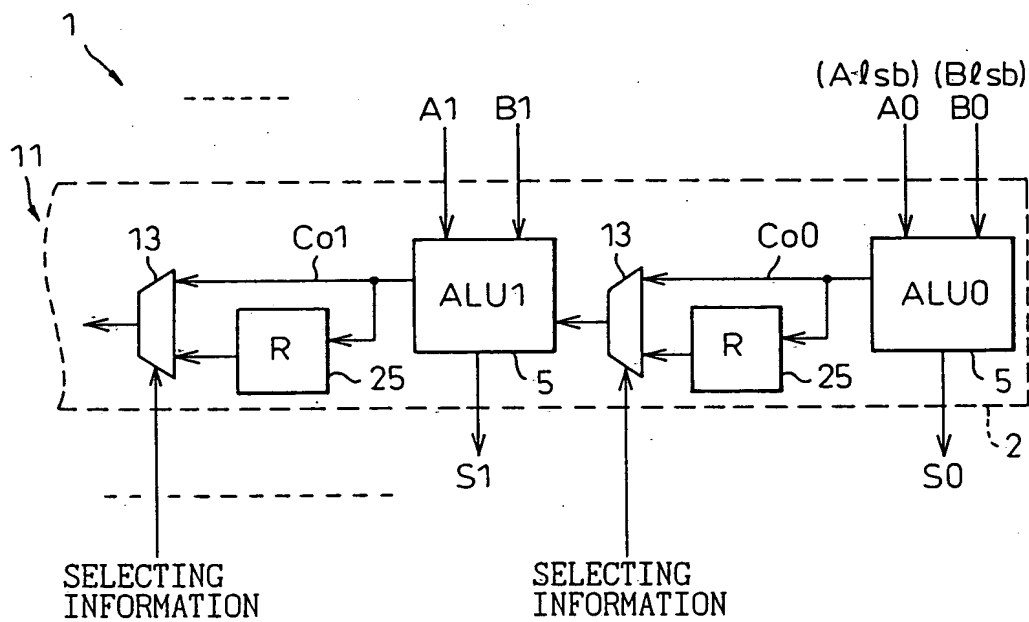


Fig.5

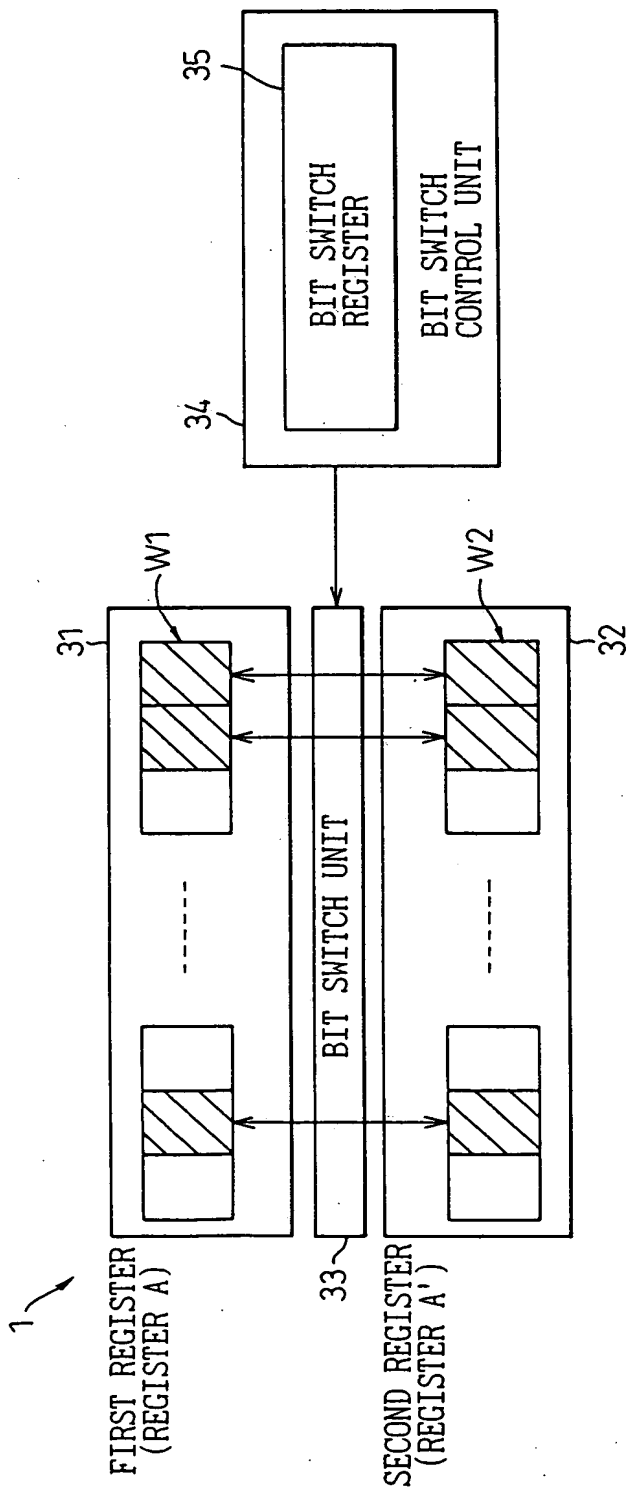


Fig.6

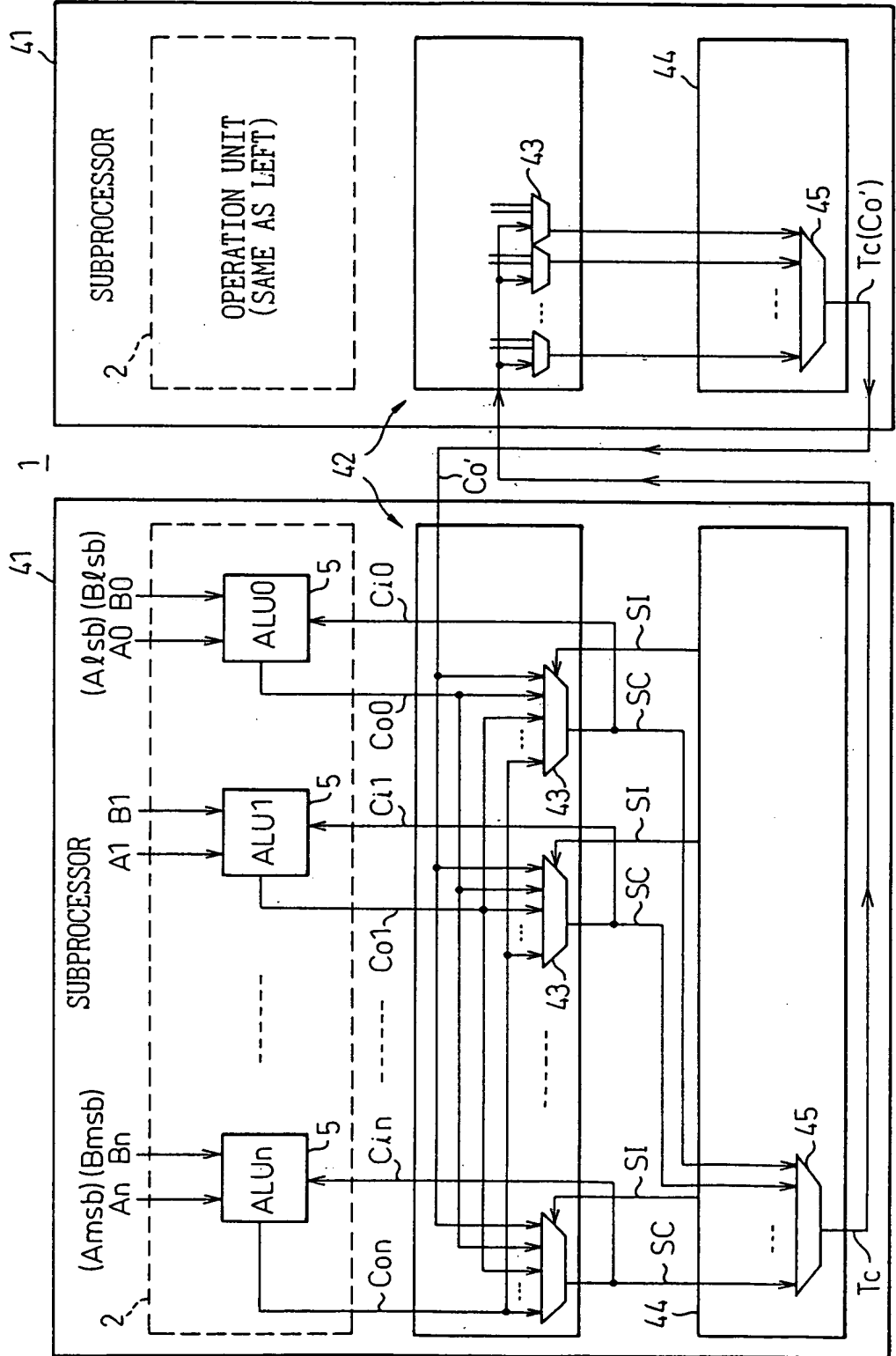
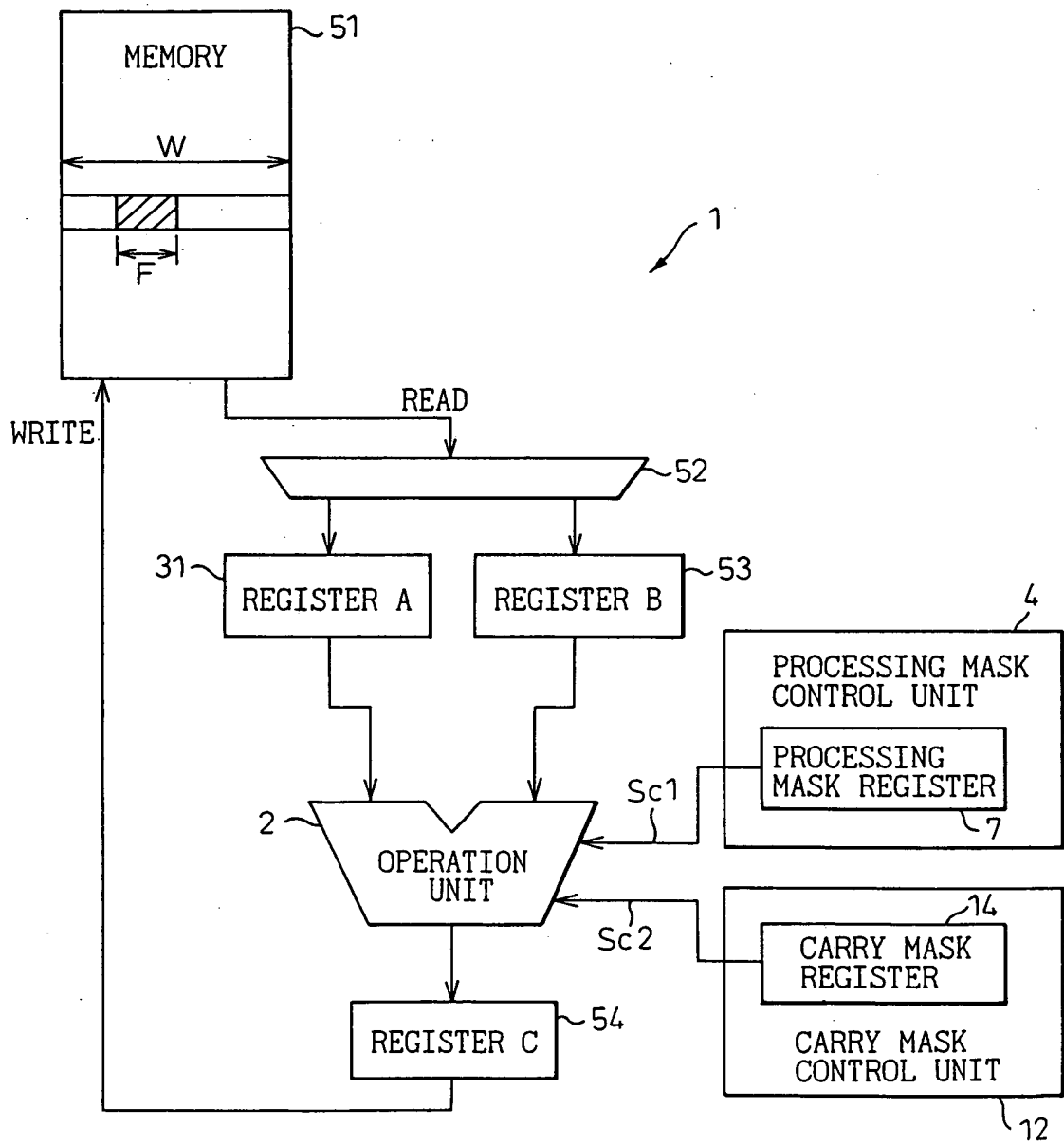


Fig. 7



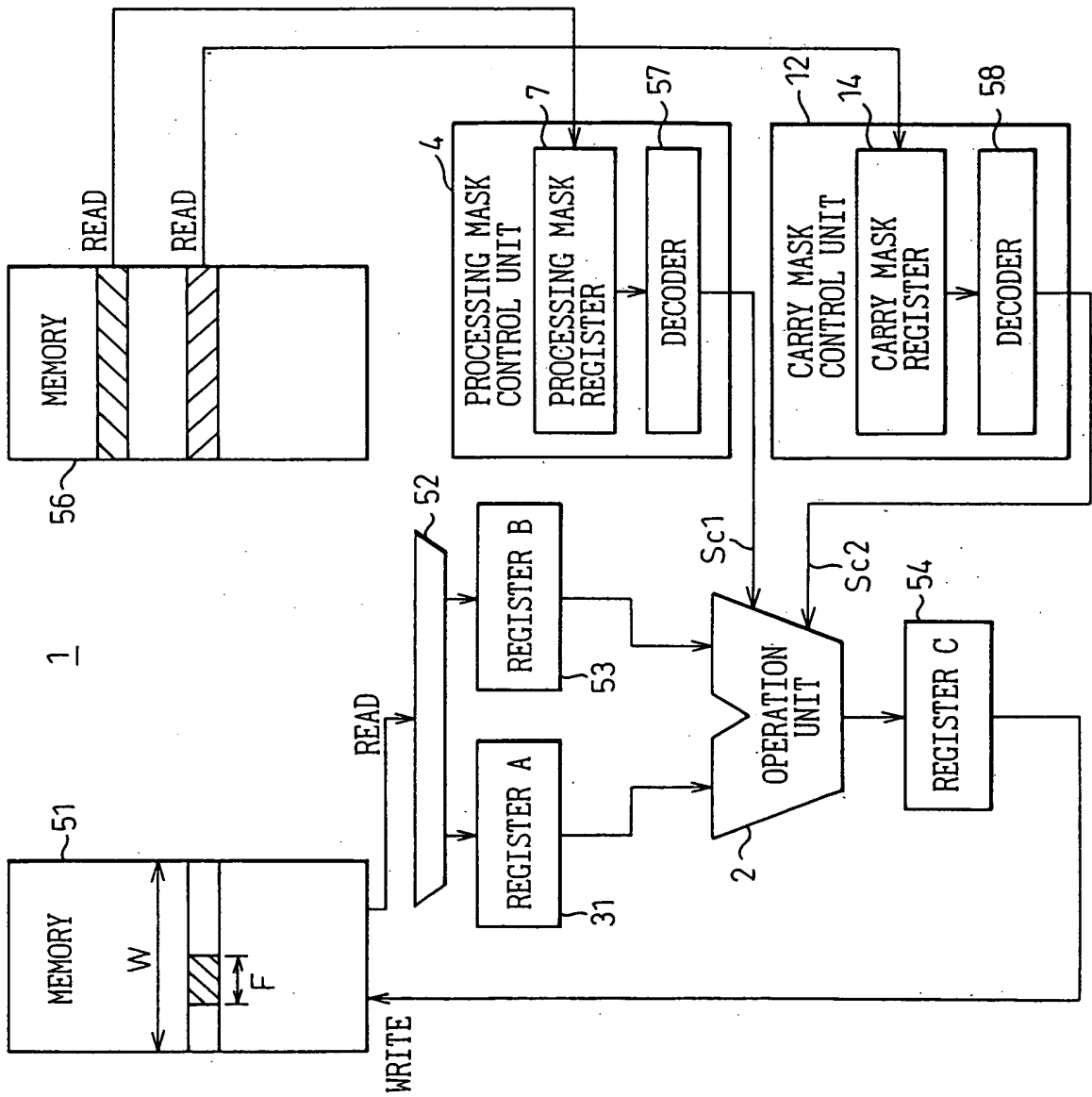


Fig. 8

Fig. 8 is a block diagram of the system of Fig. 1, showing the internal structure of the memory and the control units.



Fig. 9

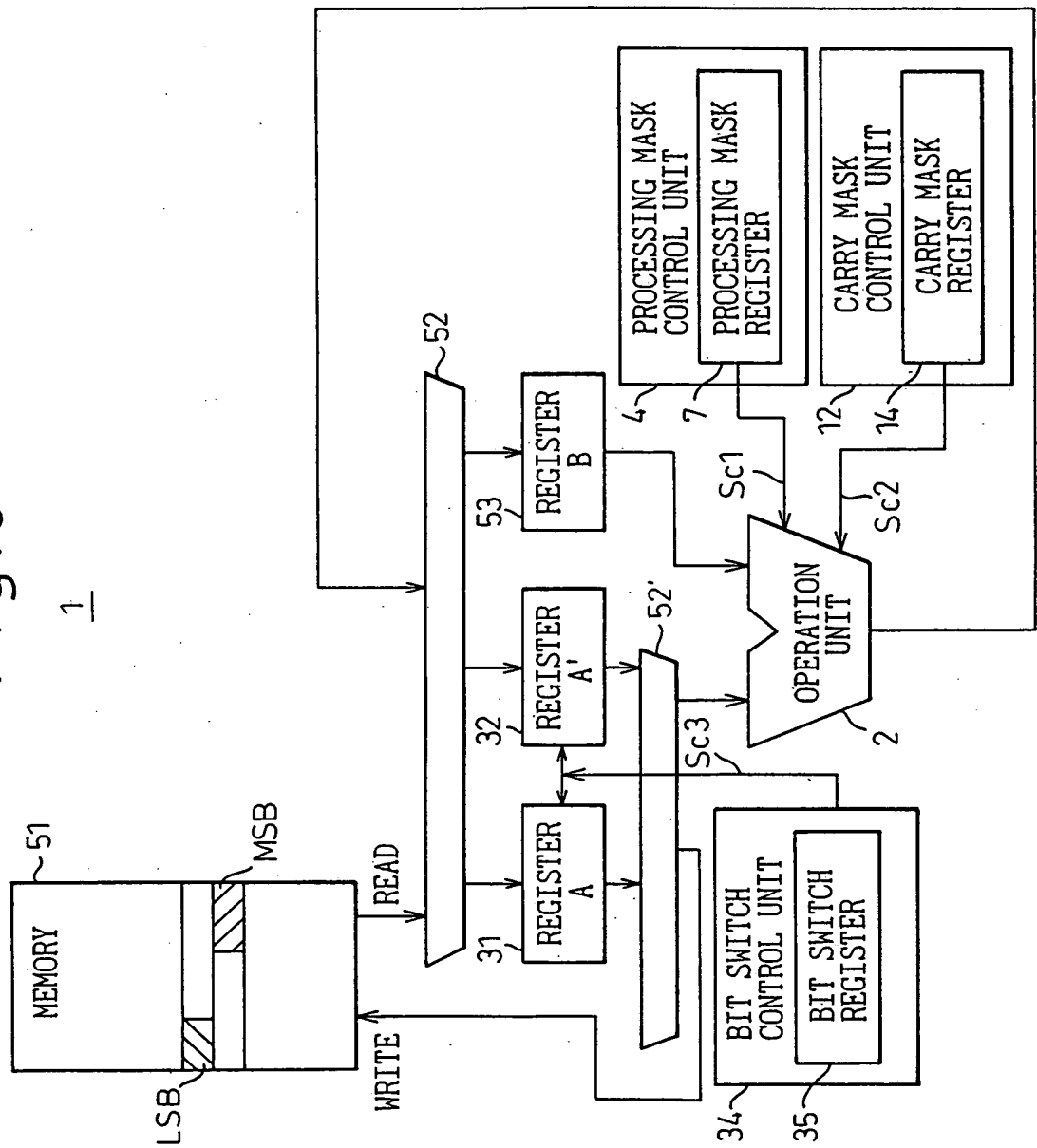


Fig.10

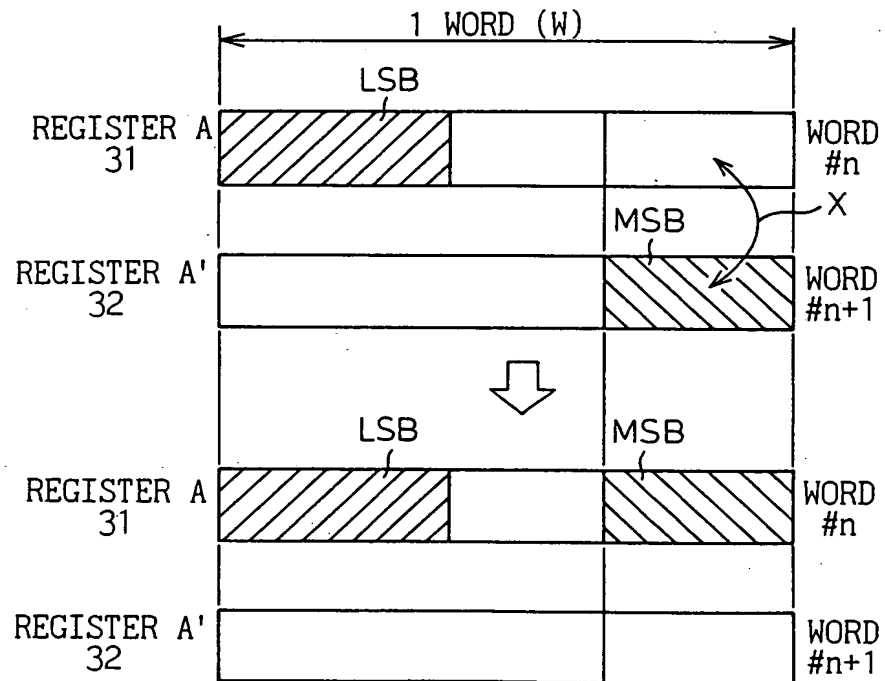


Fig.11

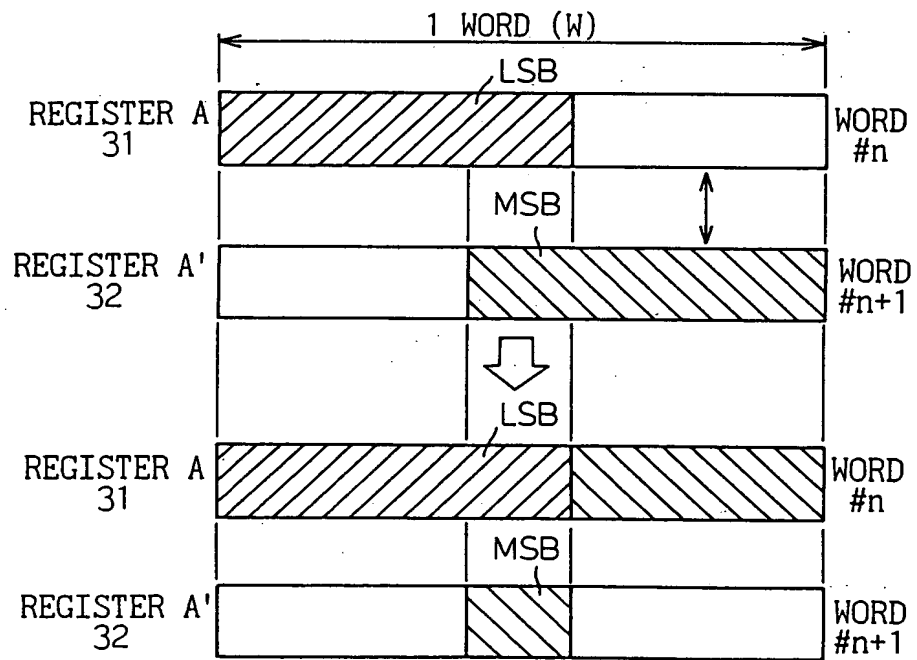


Fig. 12

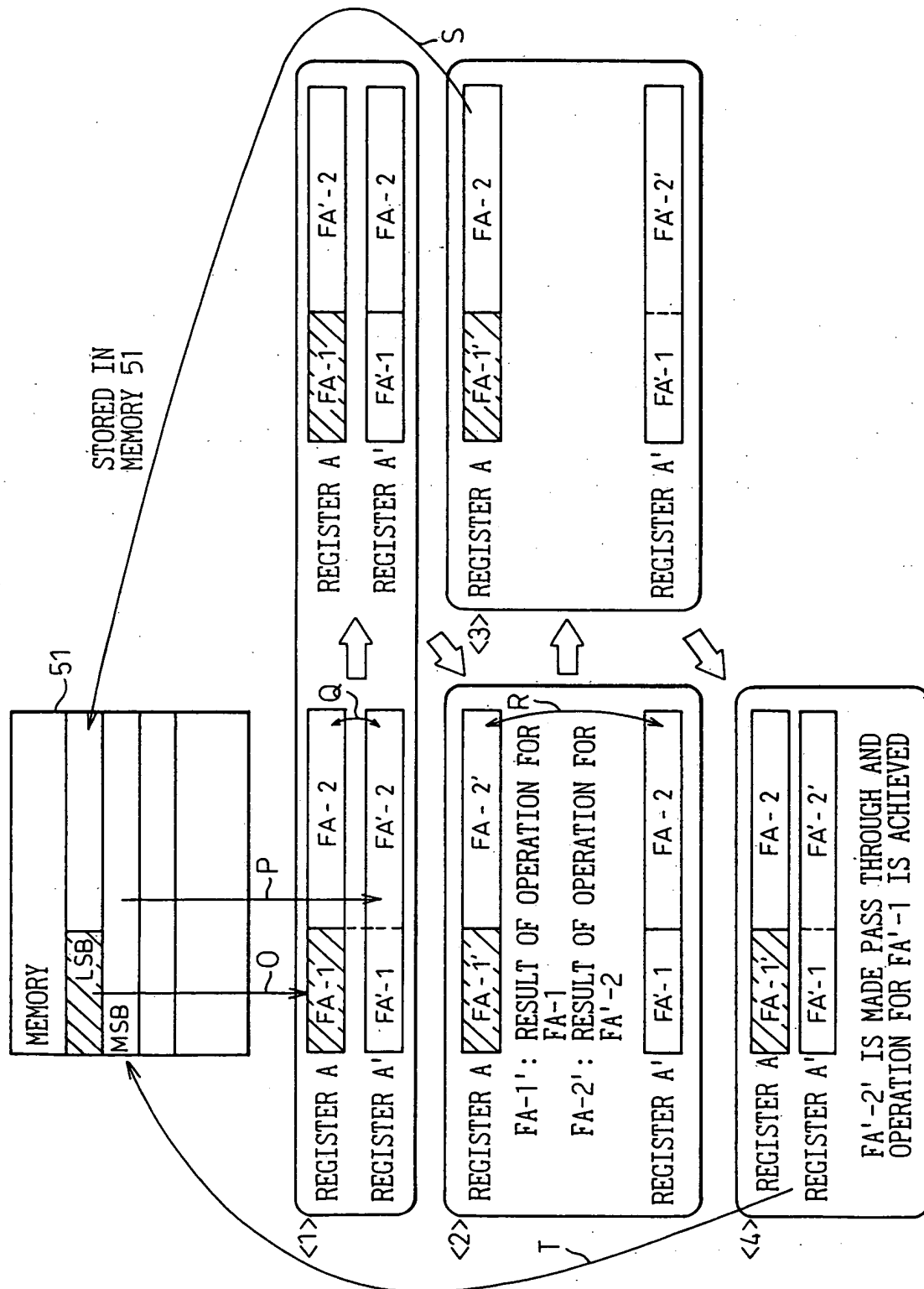


Fig.13

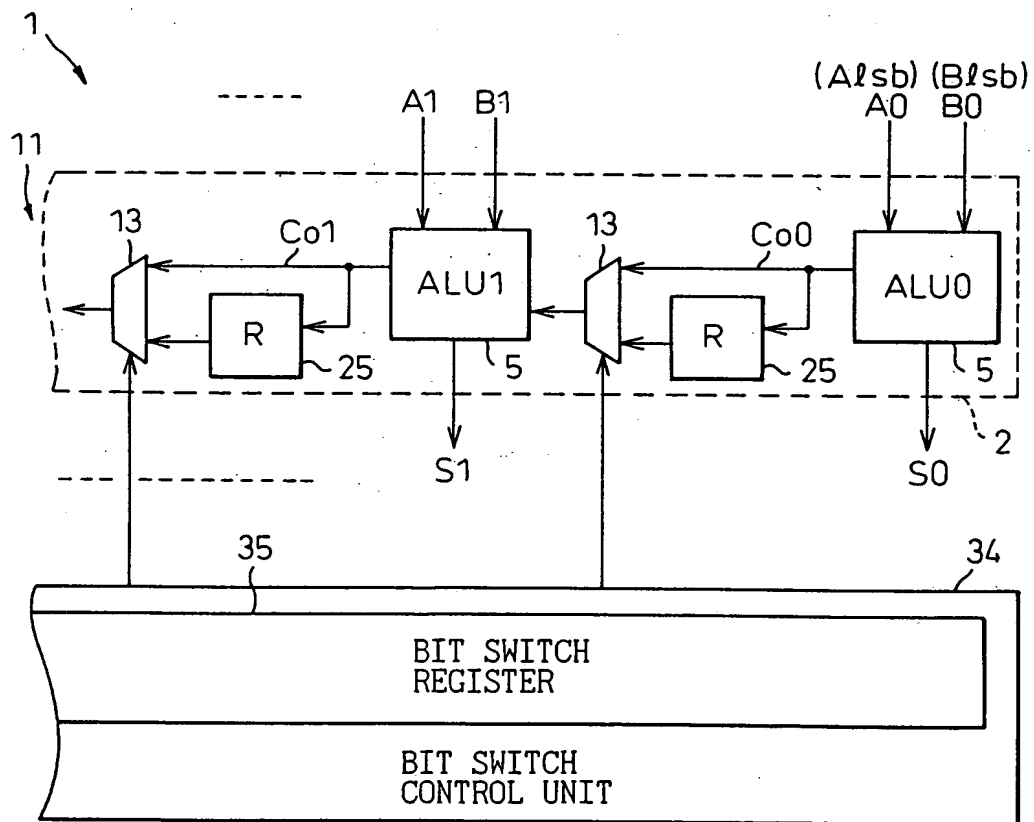


Fig.14

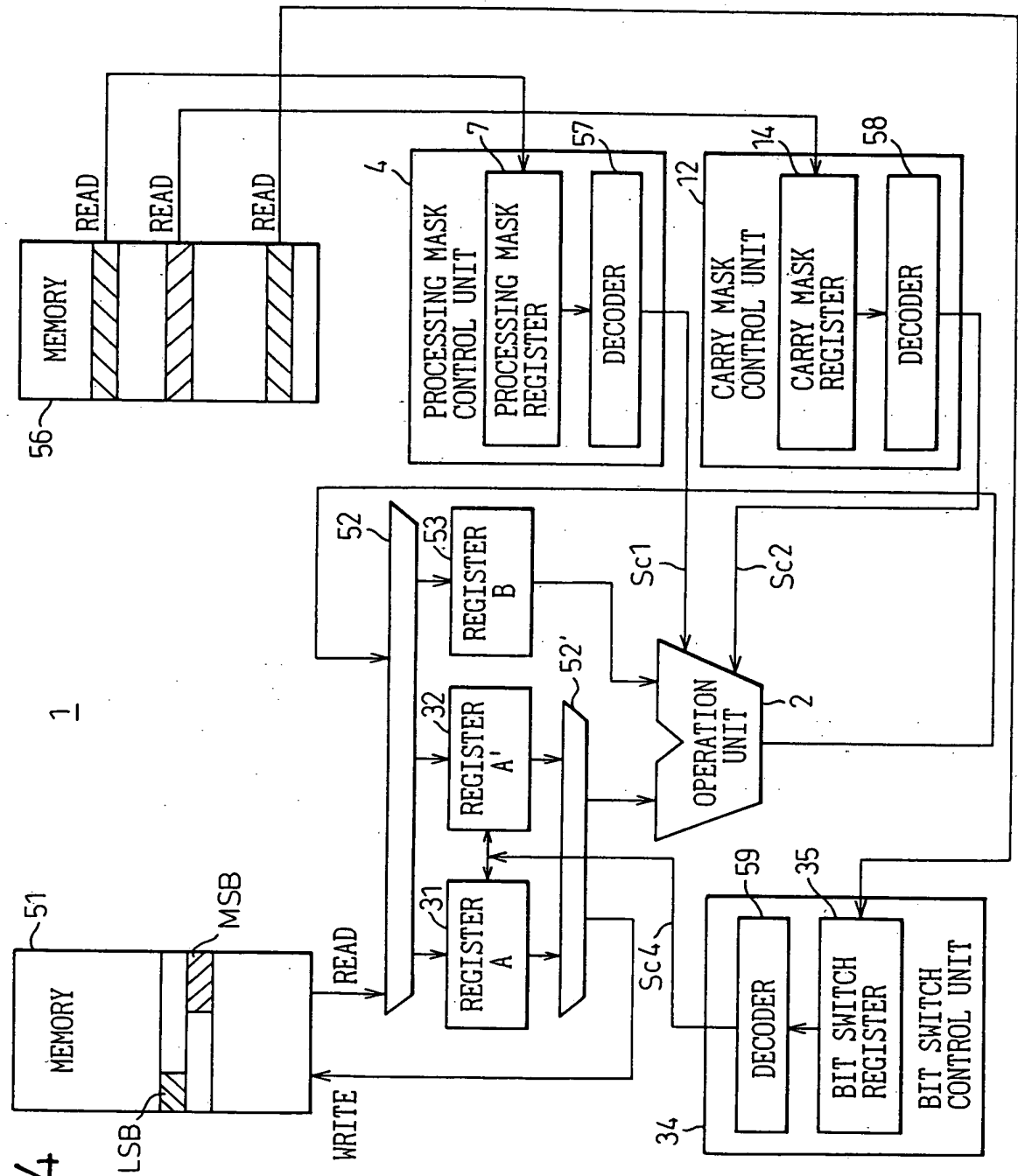


Fig.15

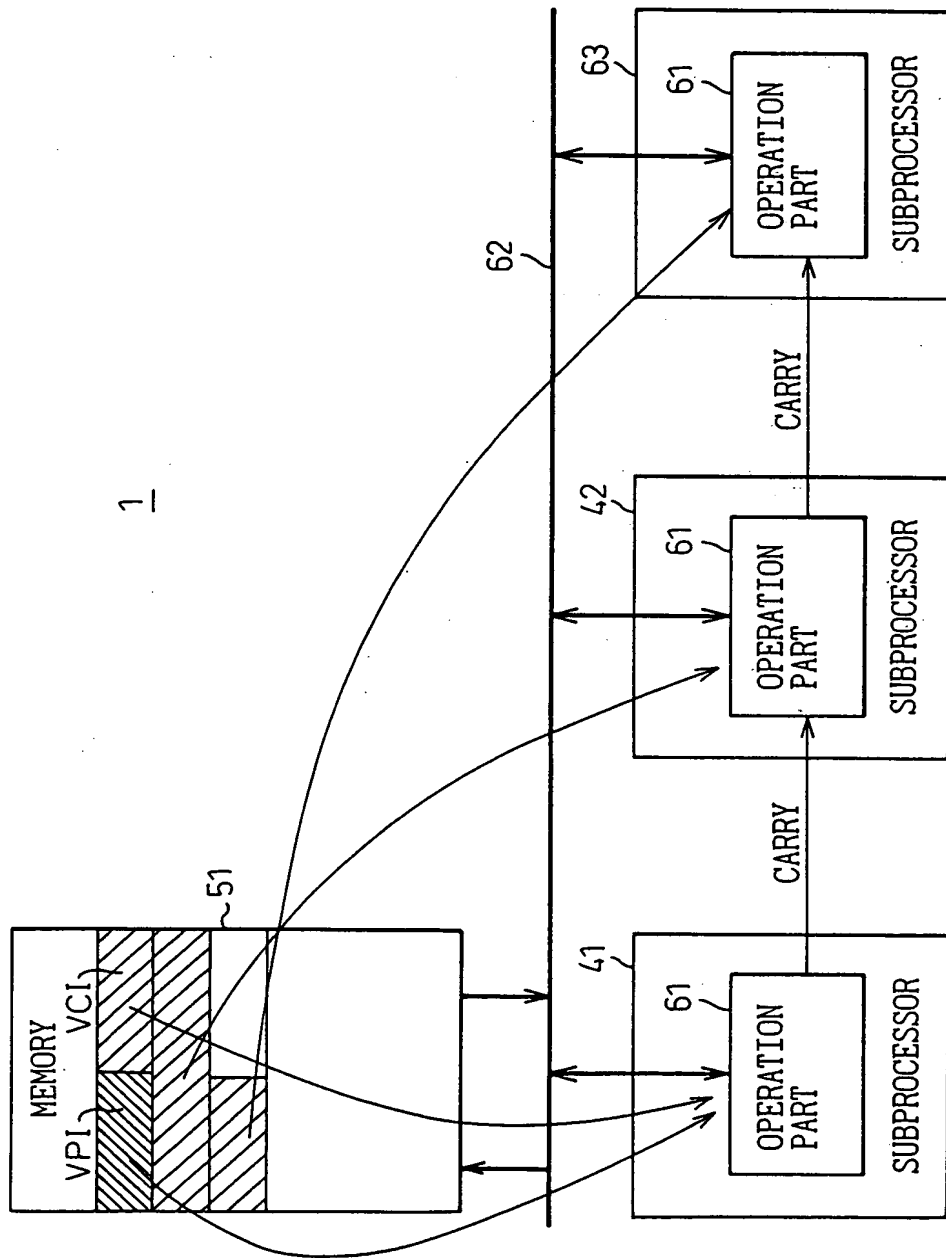


Fig.16

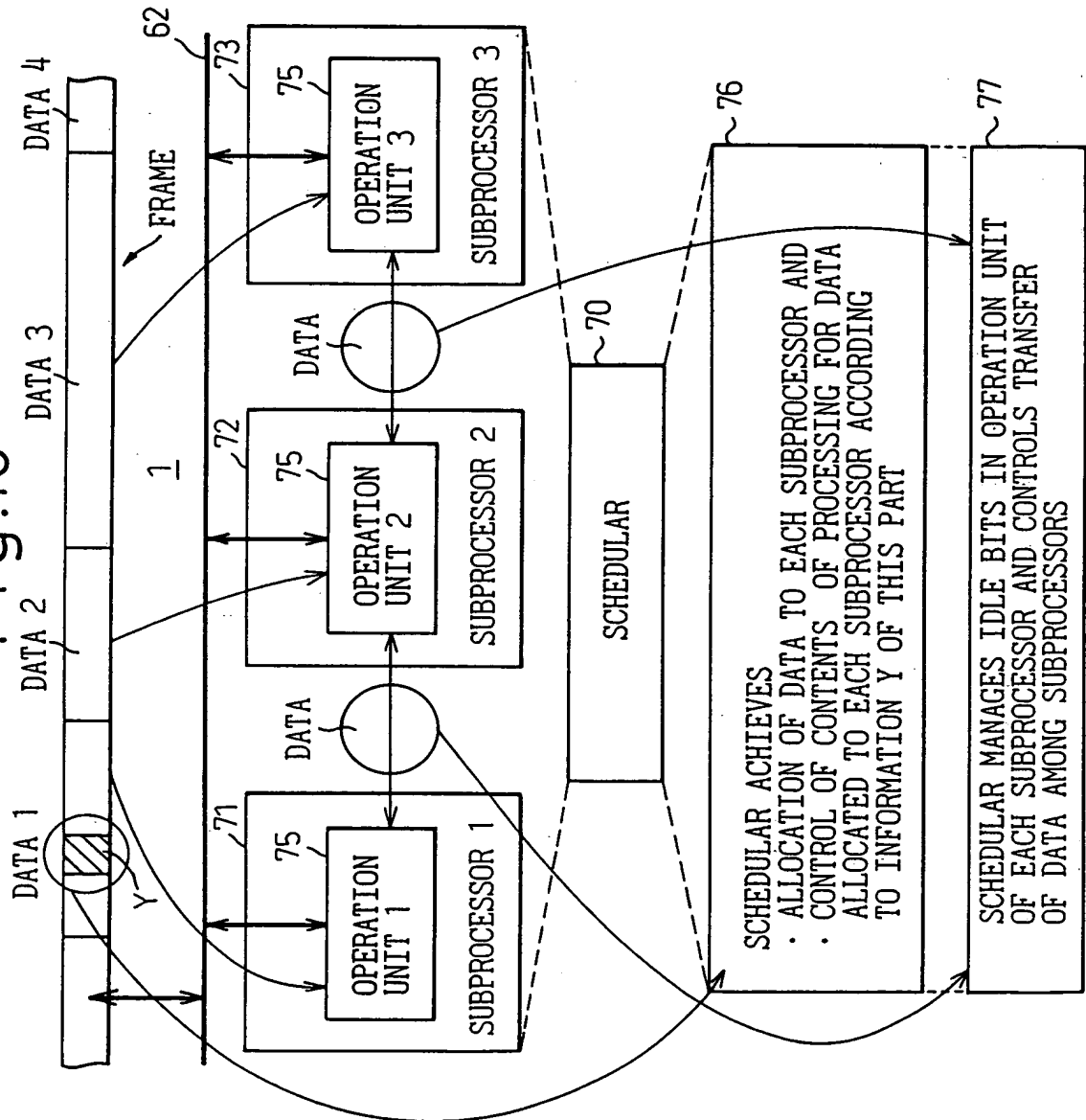




Fig.17

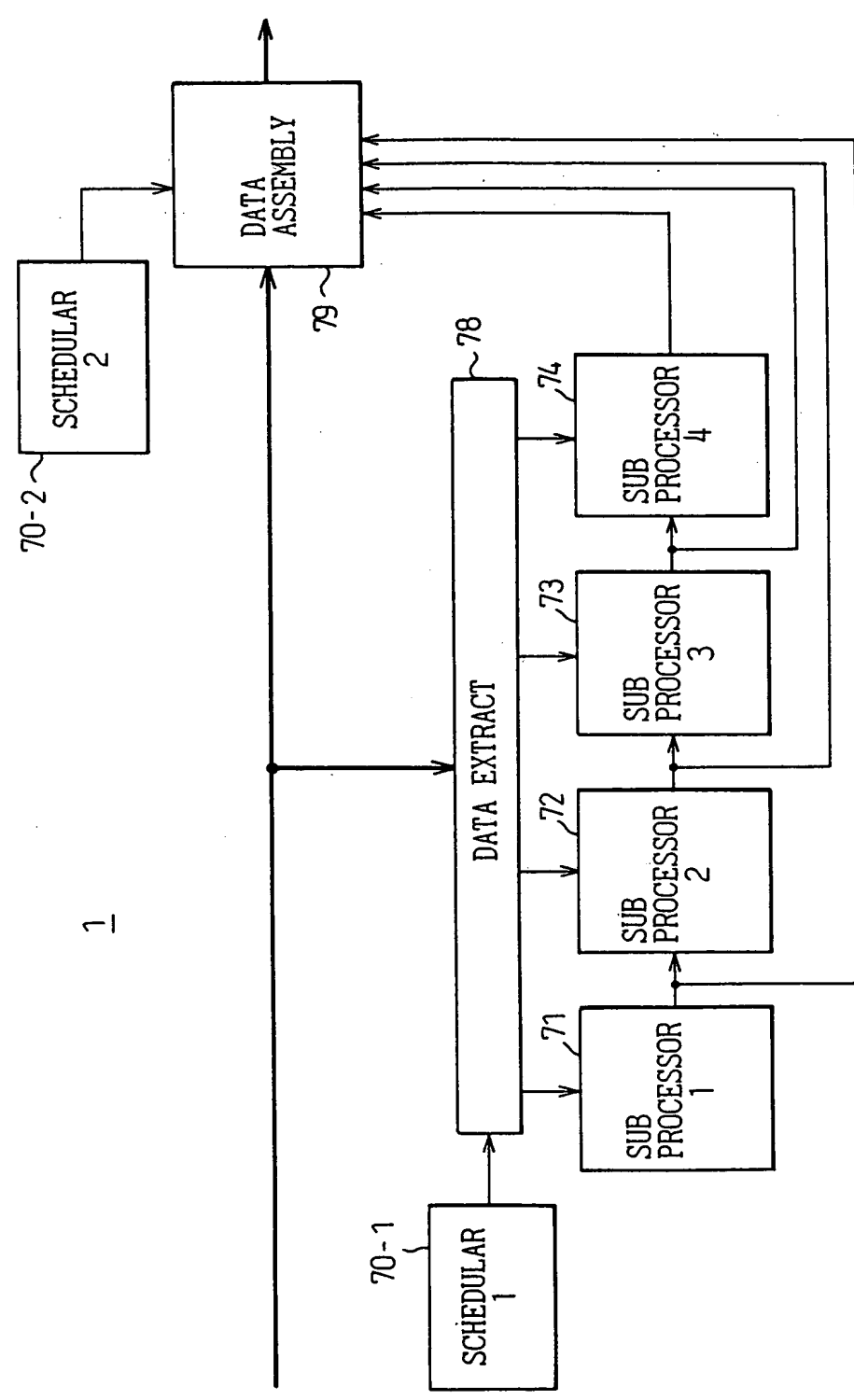


Fig.18

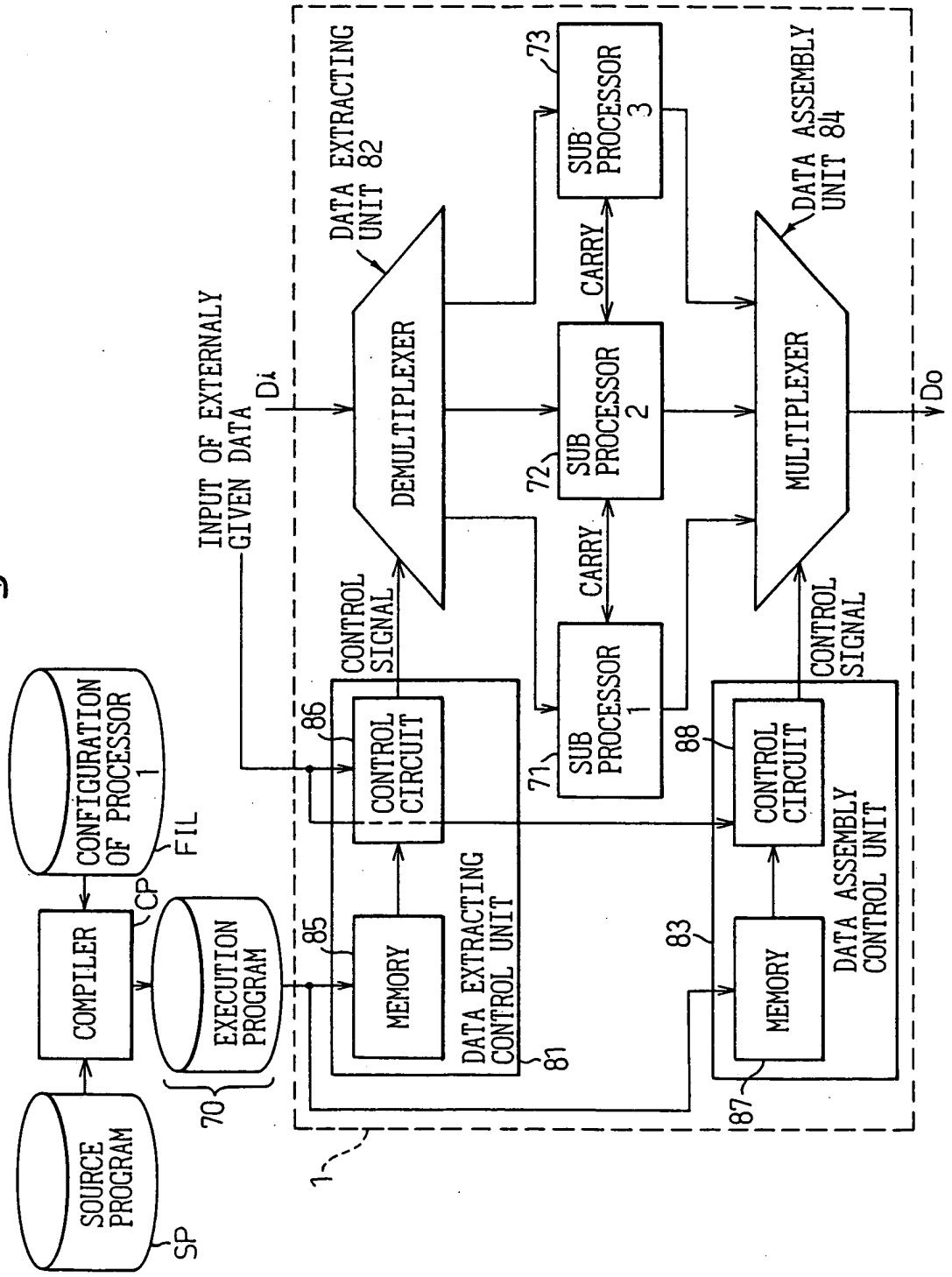
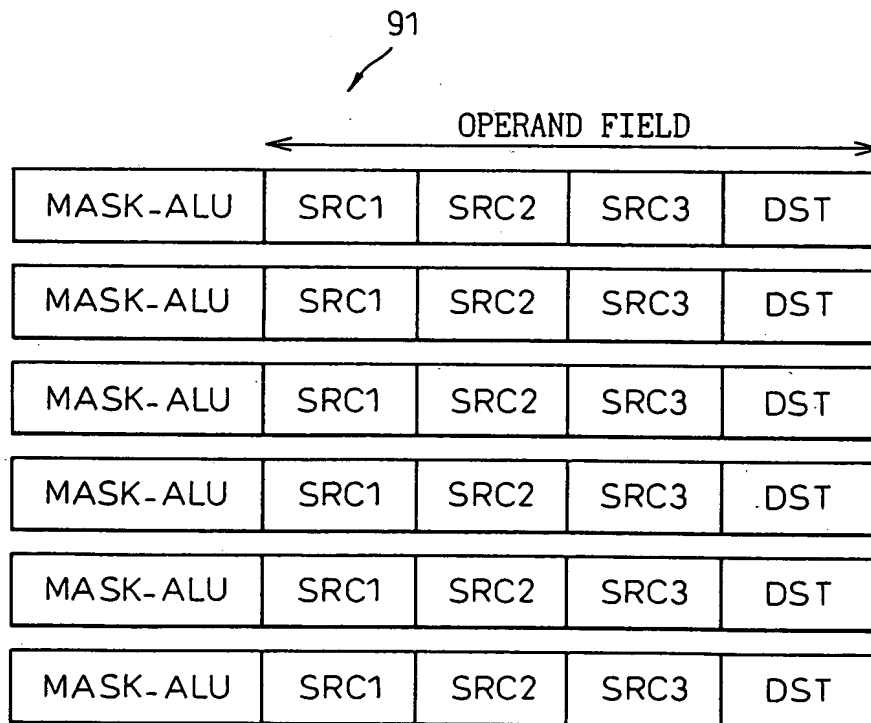
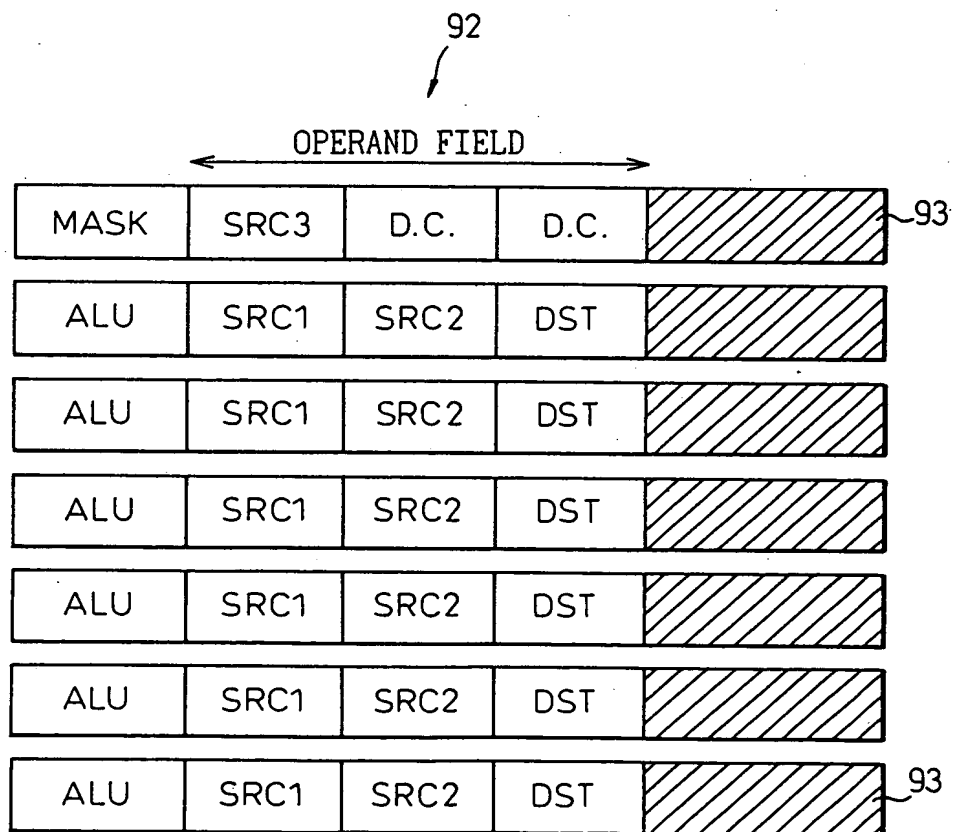


Fig.19



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Fig.20



(D.C. denotes Don't Care)